

产品规格书

Specifcation of products

产品名称:可控硅模块

产品型号: MFC110A3500VY01

浙江世菱半导体有限公司
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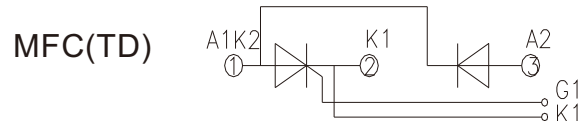
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拟制	审核	核准
林益龙	曹剑龙	宗瑞

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _j (°C)	VALUE			UNIT
				Min	Type	Max	
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Single side cooled, T _c =85°C	125			110	A
I _{T(RMS)}	RMS on-state current					173	A
V _{DRM} V _{RSM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V _{DRM} &V _{RRM} tp=10ms V _{Dsm} &V _{Rsm} = V _{DRM} &V _{RRM} +200V respectively	125		3500		V
I _{DRM} I _{RRM}	Repetitive peak current	at V _{DRM} at V _{RRM}	125			15	mA
I _{TSM}	Surge on-state current	10ms half sine wave	125			2.1	kA
I ² t	I ² t for fusing coordination	V _R =60%V _{RRM}				22	A ² s*10 ³
V _{TO}	Threshold voltage		125			1.15	V
r _T	On-state slope resistance					2.88	mΩ
V _{TM}	Peak on-state voltage	I _{TM} =330A	25			2.20	V
V _{FM}	Peak on-state voltage	I _{FM} =330A	25			1.20	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =67%V _{DRM}	125			800	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A t _r ≤0.5μs Repetitive	125			100	A/μs
I _{GT}	Gate trigger current	V _A =12V, I _A =1A	25	30		150	mA
V _{GT}	Gate trigger voltage			0.8		2.5	V
I _H	Holding current			10		200	mA
V _{GD}	Non-trigger gate voltage	V _{DM} =67%V _{DRM}	125	0.2			V
R _{th(j-c)}	Thermal resistance Junction to case	Single side cooled per chip				0.19	°C/W
R _{th(c-h)}	Thermal resistance case to heat sink	Single side cooled per chip				0.15	°C/W
V _{iso}	Isolation voltage	50Hz,R.M.S,t=1min,I _{iso} :1mA(MAX)		4000			V
F _m	Terminal connection torque (M6)				5.0		N·m
	Mounting torque (M6)				5.0		N·m
T _{vj}	Junction temperature			-40		125	°C
T _{stg}	Stored temperature			-40		125	°C
W _t	Weight				370		g
Outline							

OUTLINE DRAWING & CIRCUIT DIAGRAM



Rating and Characteristic

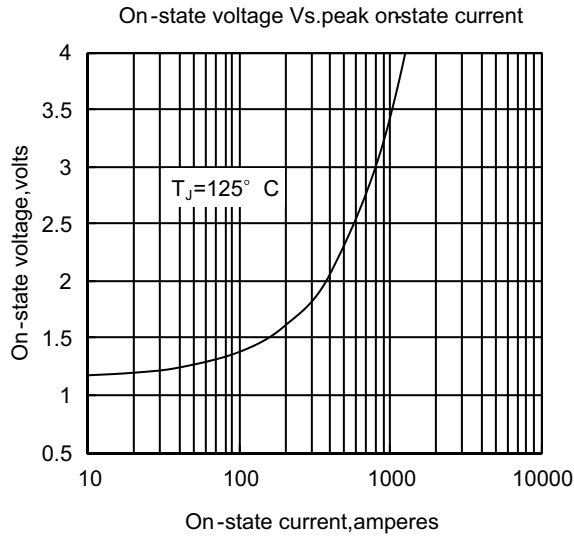


Fig. 1

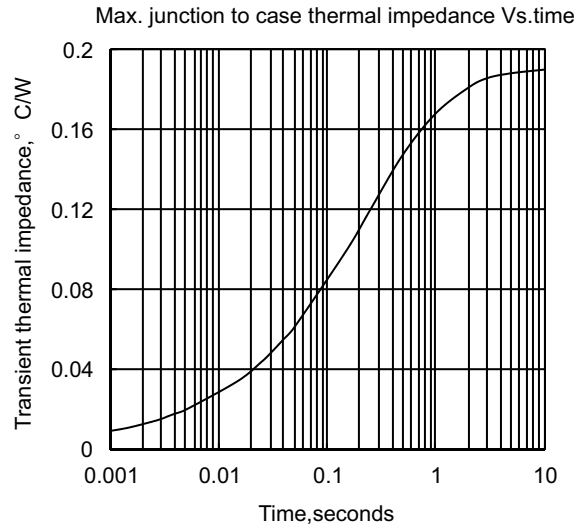


Fig. 2

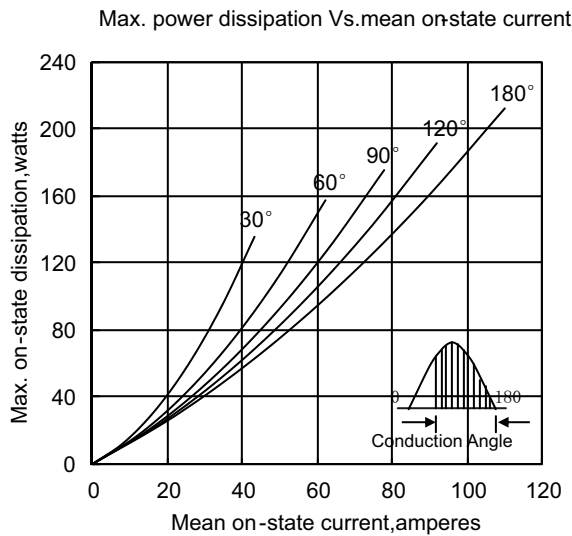


Fig. 3

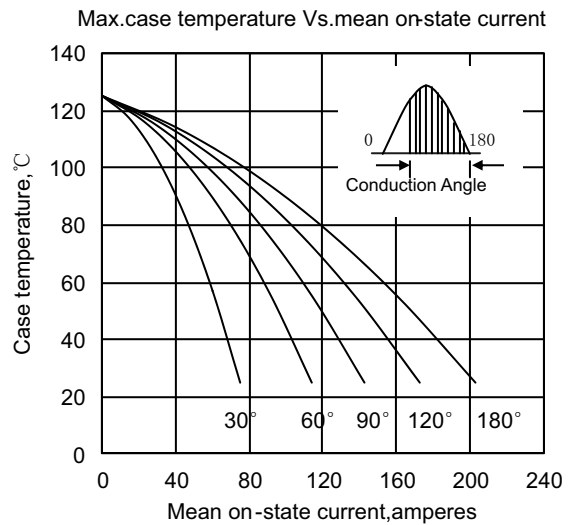


Fig. 4

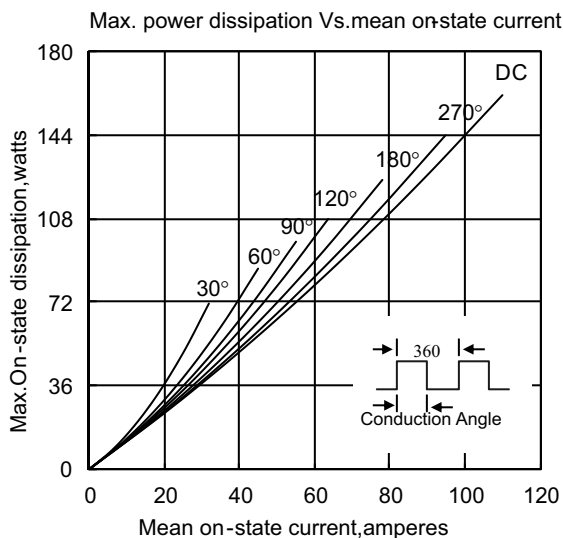


Fig. 5

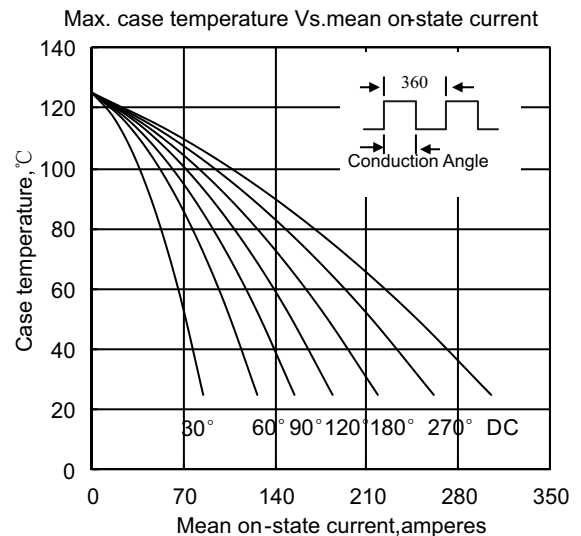


Fig. 6

Rating and Characteristic

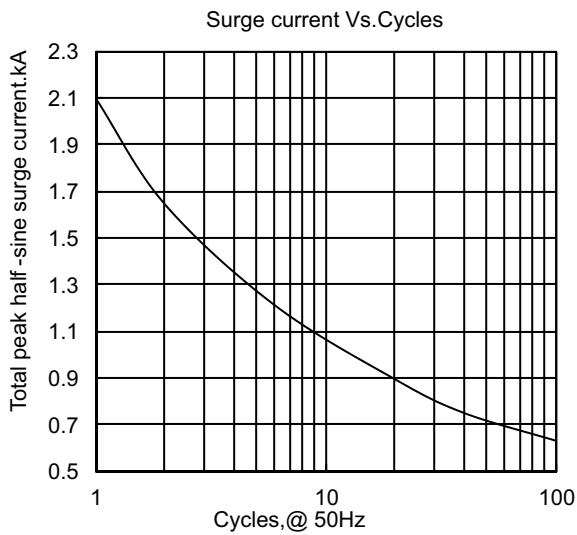


Fig. 7

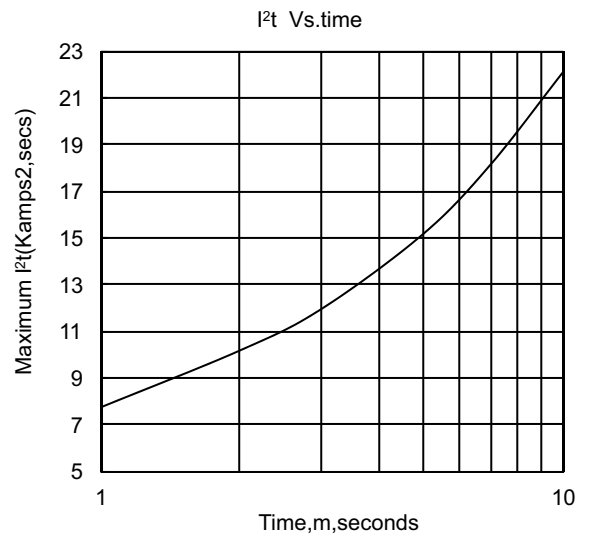


Fig. 8

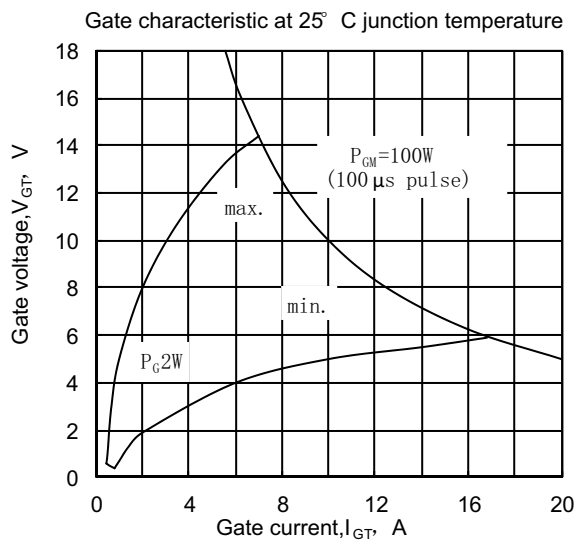


Fig. 9

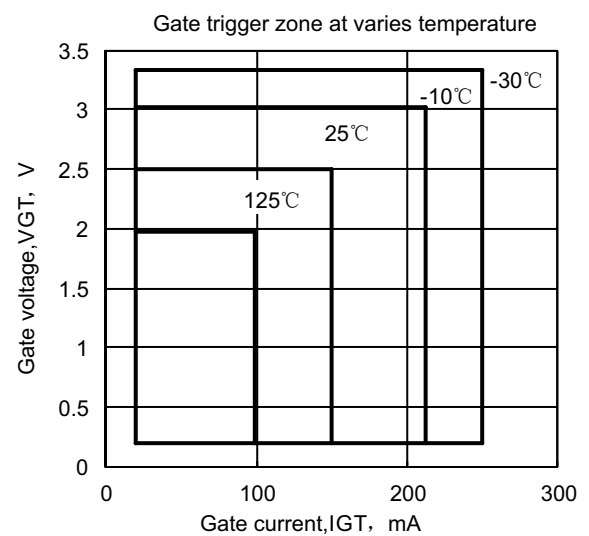


Fig. 10

Outside Dimension

