

## 产品规格书

### Specifcation of products

产品名称:可控硅模块

产品型号: MTK500A2500V-Y09

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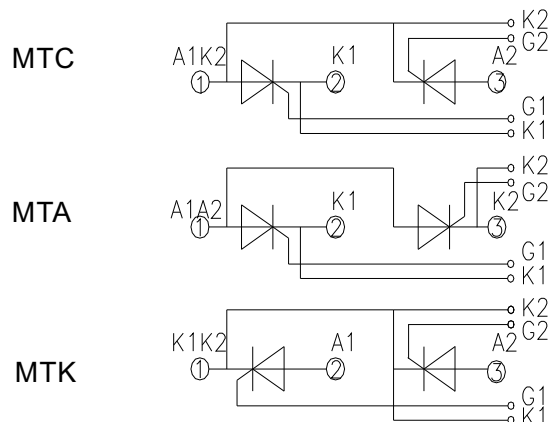
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拟制	审核	核准
林益龙	曹剑龙	宗瑞

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T <sub>j</sub> (°C)	VALUE			UNIT
				Min	Type	Max	
I <sub>T(AV)</sub>	Mean on-state current	180° half sine wave 50Hz Single side cooled, T <sub>C</sub> =85°C	125			500	A
I <sub>T(RMS)</sub>	RMS on-state current	Single side cooled, T <sub>C</sub> =85°C	125			785	A
V <sub>DRM</sub> V <sub>RRM</sub>	Repetitive peak off-state voltage Repetitive peak reverse voltage	V <sub>DRM</sub> &V <sub>RRM</sub> tp=10ms V <sub>DSM</sub> &V <sub>RSM</sub> = V <sub>DRM</sub> &V <sub>RRM</sub> +200V respectively	125		2500		V
I <sub>DRM</sub> I <sub>RRM</sub>	Repetitive peak current	at V <sub>DRM</sub> at V <sub>RRM</sub>	125			40	mA
I <sub>TSM</sub>	Surge on-state current	10ms half sine wave	125			16.0	KA
I <sup>2</sup> t	I <sup>2</sup> T for fusing coordination	V <sub>R</sub> =60%V <sub>RRM</sub>				1310	A <sup>2</sup> s*10 <sup>3</sup>
V <sub>TO</sub>	Threshold voltage		125			0.80	V
r <sub>T</sub>	On-state slop resistance					0.34	mΩ
V <sub>TM</sub>	Peak on-state voltage	I <sub>TM</sub> =1500A	125			1.5	V
dv/dt	Critical rate of rise of off-state voltage	V <sub>DM</sub> =67%V <sub>DRM</sub>	125			800	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V <sub>DRM</sub> to 1500A, Gate source 1.5A t <sub>r</sub> ≤ 0.5 μs Repetitive	125			300	A/μs
I <sub>GT</sub>	Gate trigger current			30		200	mA
V <sub>GT</sub>	Gate trigger voltage	V <sub>A</sub> =12V, I <sub>A</sub> =1A	25	1.0		3.0	V
I <sub>H</sub>	Holding current			20		100	mA
V <sub>GD</sub>	Non-trigger gate voltage	At 67%V <sub>DRM</sub>	125			0.2	V
R <sub>th(j-c)</sub>	Thermal resistance Junction to heatsink	At 180° sine Single side cooled				0.065	°C /W
V <sub>iso</sub>	Isolation voltage	50Hz, RMS, t=1min, I <sub>iso</sub> : 1mA (MAX)		3000			V
F <sub>m</sub>	Thermal connection torque (M10)				9.0		N.m
	Mounting torque (M6)				5.0		N.m
T <sub>stg</sub>	Stored temperature			-40		140	°C
W <sub>t</sub>	Weight				1481		g
Outline							

### OUTLINE DRAWING & CIRCUIT DIAGRAM



### Rating and Characteristic

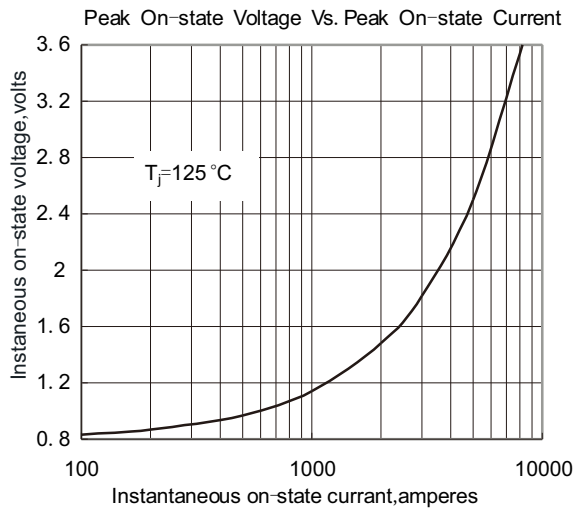


Fig. 1

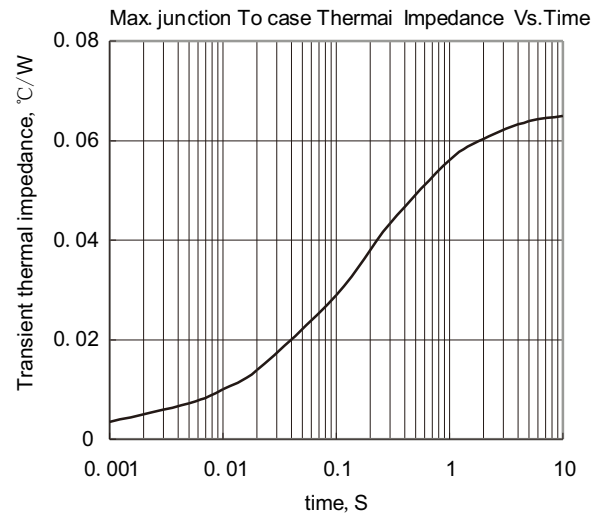


Fig. 2

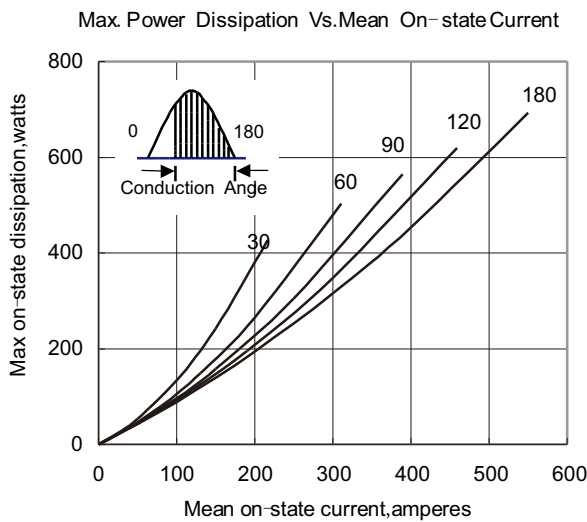


Fig. 3

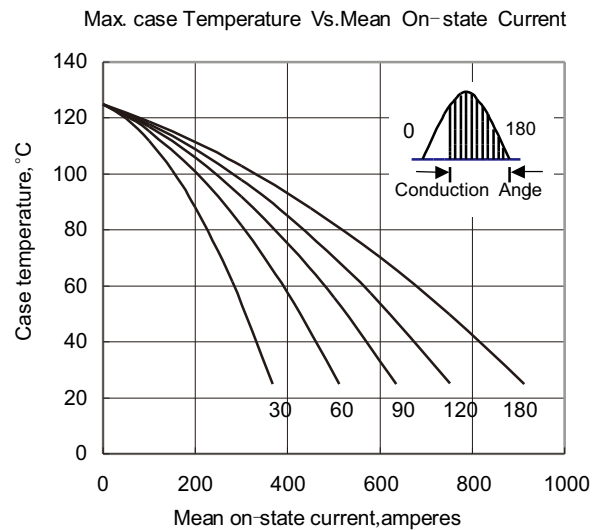


Fig. 4

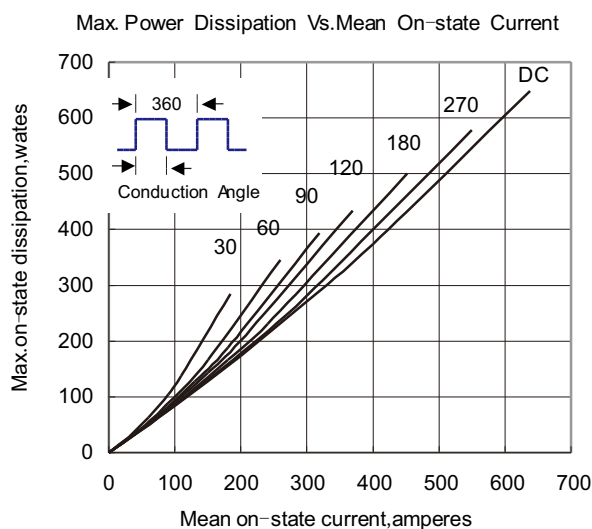


Fig. 5

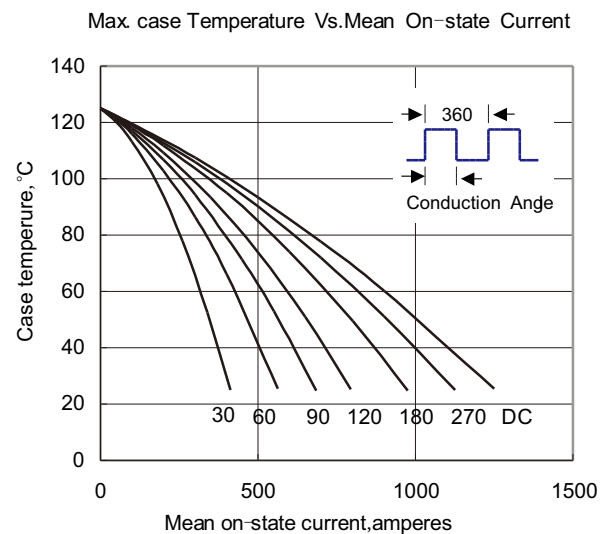


Fig. 6

### Rating and Characteristic

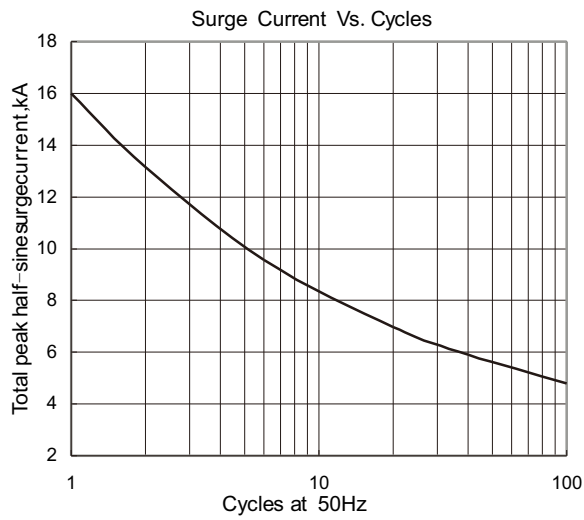


Fig. 7

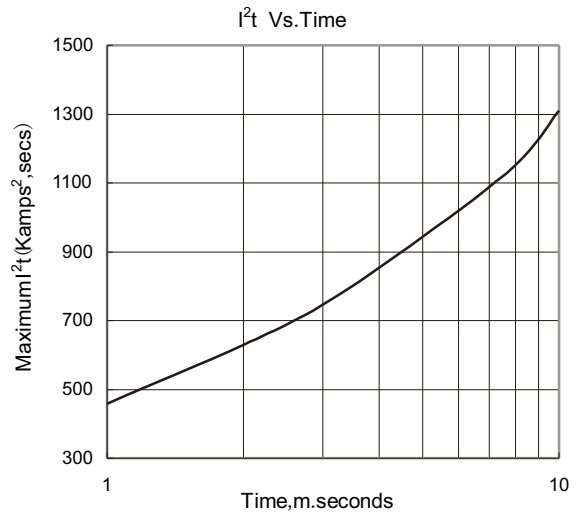


Fig. 8

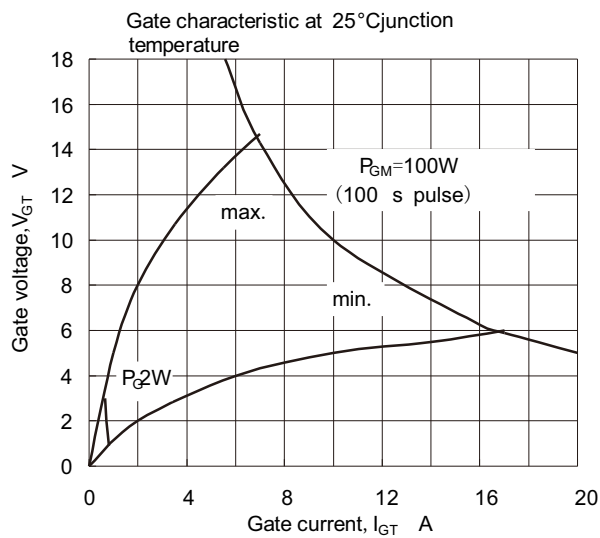


Fig. 9

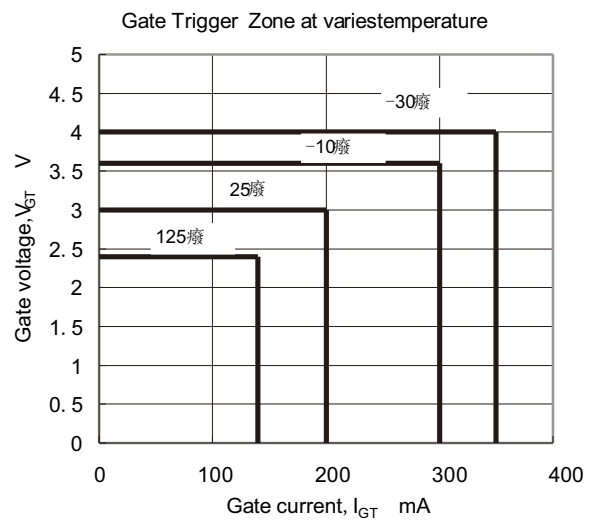


Fig. 10

## Outside Dimension

